

ABSTRACT OF THE DISCLOSURE

A multi-port semiconductor memory in which wrong read-out due to coupling noise is hardly generated and operation speed is fast is provided. When data are written in memory cells from a pair of bit lines for one port, NMOS transistors become on. Electrical potential only at a low-level side is pulled up between the pair of bit lines, because electrical potential at a high-level side is approximately equivalent to power potential. Accordingly, when one of adjacent bit lines is on high-level and the other is on low-level, potential difference is reduced by the pull-up, resulting in reduction of generating time of the coupling noise. Although read-out of data can not be performed while the coupling noise is being generated, since the concerned generating time is reduced in the invention, the operation speed is substantially fast.